International Symposium on Networks-on-Chip

Call for Papers

12th IEEE/ACM International Symposium on Networks-on-Chip
October 4~5, 2018, Torino, Italy
(*Co-located with Embedded Systems Week 2018*)

The International Symposium on Networks-on-Chip (NOCS) is the premier event dedicated to interdisciplinary research on on-chip, package-scale, and rack-scale communication technology, architecture, design methods, applications and systems. NOCS brings together scientists and engineers working on NoC innovations and applications from inter-related research communities, including discrete optimization and algorithms, computer architecture, networking, circuits and systems, packaging, embedded systems, and design automation. Topics of interest include, but are not limited to:

NoC Architecture and Implementation
- Network architecture (topology, routing, arbitration)
- Timing, synchronous/asynchronous communication
- NoC reliability issues and solutions
- Power and thermal issues at the NoC un-core and system-level
- Network interface issues and solutions
- Signaling & circuit design for NoC links and routers

NoC and Communication Analysis, Optimization, and Verification
- NoC performance analysis and Quality of Service
- Modeling, simulation, and synthesis of NoC
- Verification, debug and test of NoC
- NoC design and simulation methodologies and tools
- Metrics, benchmarks, and experiences on NoC-based hardware
- Communication efficient algorithms
- Communication workload characterization & evaluation

Novel NoC Technologies
- Optical, wireless, carbon nanotube, and other emerging technologies
- NoC for 3D and 2.5D packages
- Package-specific NoC design
- Network coding and compressed solutions for efficient terabyte NoC architectures
- Approximate computing for NoC and NoC-based systems

NoC for Intelligent Physical Systems
- Mapping of existing and emerging applications onto NoC
- NoC case studies, application-specific NoC design
- NoC for FPGA, structured ASIC, CMP and MPSoC
- NoC designs for heterogeneous systems, fused CPU-GPU and data-center-on-a-chip (DCoC) architectures
- Scalable modeling of NoC
- Machine learning for NoC and NoC-based Systems

NoC at the Un-Core and System-level
- Design of memory subsystem (un-core) including memory controllers, caches, cache coherence protocols in NoC
- In-memory/In-storage network and NoC for new memory/storage technologies
- NoC support for memory and cache access
- OS support for NoC
- Security issues and solutions in NoC architectures
- Programming models including shared memory, message passing and novel programming models
- Issues related to large-scale systems (datacenters, supercomputers, edge and fog computing) with NoC-based systems as building blocks

Inter/Intra-Chip and Rack-Scale Network
- Unified inter/intra-chip networks
- Hybrid chip-scale and rack-scale networks
- All aspects of inter-chip network design
- All aspects of rack-scale network design

Electronic paper submission requires a full paper, up to 8 double-column IEEE format pages, including figures and references. The program committee in a double-blind review process will evaluate papers based on scientific merit, innovation, relevance, and presentation. *Submitted papers must describe original work that has not been published before or is under review by another conference or journal at the same time*. Each submission will be checked for any significant similarity to previously published works or for simultaneous submission to other archival venues, and such papers will be rejected. Proposals for special sessions and demos are invited. Paper submissions and demo proposals by industry researchers or engineers to share their experiences and perspectives are also welcome. A percentage of accepted papers will be recommended for publication in IEEE Transactions on Multi-Scale Computing Systems after revision according to the review comments. Please find the detailed submission instructions for paper submissions, special session, and demo proposals at the submission page. Further information is available via:

www.nocs2018.conf.kth.se

Important Dates (Anywhere on Earth)

Abstract registration deadline	~~**April 24**~~ **May 8, 2018**	Notification of acceptance	**July 1, 2018**
Full paper submission deadline	~~**May 1**~~ **May 15, 2018**	Final version due	**July 15, 2018**

General Chairs
Zhonghai Lu (KTH Royal Institute of Technology)
Sriram Vangal (Intel Corporation)
Web Chair
Akram Ben Ahmed (Keio University)
Publicity Chairs
Edoardo Fusella (University of Naples Federico II)
Tushar Krishna (Georgia Institute of Technology)
Chun-Yi Lee (National Tsing Hua University)
Steering Committee Chair
Radu Marculescu (Carnegie Mellon University)

Technical Program Chairs
Paul Bogdan (University of Southern California)
Jiang Xu (Hong Kong University of Science and Technology)
Publication Chair
Vassos Soteriou (Cyprus University of Technology)
Special Session/Tutorial Chairs
Maurizio Palesi (University of Catania)
Amlan Ganguly (Rochester Institute of Technology)
Local Arrangements Chair
Mario Casu (Politecnico di Torino)
Finance Chair
Turbo Majumder (Intel Corporation)